

Woonhyun Nam

CONTACT INFORMATION Computer Vision Lab. *Tel:* +82-54-279-2916
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OBJECTIVE Software engineer developing large-scale and/or real-time systems based on computer vision and machine learning techniques (e.g., multi-class object detection, object segmentation, object tracking, and image categorization; representation learning and relational feature learning)

EDUCATION **Pohang University of Science and Technology (POSTECH)**, Korea, Republic of

Ph.D., Computer Science and Engineering, February 2014

- Thesis Topic: *Pedestrian Detection and Localization by Learning Local Macro-features*
- Adviser: Professor Joon Hee Han
- Area of Study: Computer Vision
- GPA: 4.09 / 4.3

B.E., Computer Science and Engineering, February 2005

- *Magna cum Laude*
- GPA: 3.66 / 4.3

TECHNICAL SKILLS **Embedded and Real-time Systems:**

- Software development with Texas Instruments DSP platforms (e.g., DM64x)
- Fixed-point implementation and code optimization for DSP

GPU Computing:

- Software development with NVIDIA CUDA architectures
- Profiling and code optimization for CUDA

Programming Languages:

- C, C++, CUDA, Matlab, Java, Python, Verilog, HTML, PHP, SQL, and others

Server Administration:

- A 6-node Centos cluster and workstations

RESEARCH EXPERIENCE **Pohang University of Science and Technology (POSTECH)**, Korea, Republic of

Research Assistant **2006-Present**
(9 industrial research projects; PI: Professor Joon Hee Han)

Pedestrian Detection 2010-Present

- Introduced new feature representations and their learning method for accurate object localization. Developed, implemented, and evaluated an efficient pedestrian detection algorithm based on the representations.

- Accelerated the detection algorithm using CUDA; 1 ch 100+ fps and 10 ch 10+ fps for 640x480 images.
- Recent research has achieved more than 10%p higher detection rate than state-of-the-art algorithms on a challenging dataset.

Moving Object Segmentation

2006-2011, and 2013

- Developed and implemented an efficient moving object segmentation algorithm using a static camera, which utilized temporal locality of image observations by using LRU scheduling for background model matching and update. The algorithm runs at more than 200 fps for 360x240 images using a 2.13 GHz CPU.
- Collaborated on the development of object detection functionality for intelligent IP cameras and air conditioners; ported the algorithm to a TI DSP and optimized the DSP code. It was accelerated 7.6 times faster than before.
- Extended the algorithm to a moving camera in cooperation with lab colleagues.
- Have developed a supervised learning framework for moving object segmentation based on background likelihoods and other features.

Object Tracking

2006 and 2010-2011

- Developed, implemented, and evaluated a real-time multi-target tracking and recognition system in cooperation with lab colleagues.
- Developed, implemented, and evaluated a real-time multi-person tracking system which integrated pedestrian detection algorithm with the multi-target tracking system developed previously.
- Developed, implemented, and evaluated an occlusion reasoning algorithm for object tracking in cooperation with lab colleagues.

Depth Estimation in Stereo Vision

2006

- Implemented a depth estimation algorithm using stereo matching.
- Collaborated on the development of a 3D reconstruction system for realistic modeling of golf courses.

TEACHING EXPERIENCE

Pohang University of Science and Technology (POSTECH), Korea, Republic of

Teaching Assistant

2005 and Fall 2007

Lab Instructor for CSED 312: Operating Systems

Fall 2007

- Responsible for designing, supervising, and grading one of four laboratory projects. Students implemented operating system functionality for kernel threads, user programs, virtual memory, and file systems using **Pintos**.

Assistant for CSED 341: Automata and Formal Languages

Fall 2005

- Responsible for developing mathematical problem-solving skills for students.

Lab Instructor for CSED 313: Computer Architecture Laboratory

Spring 2005

- Responsible for designing, supervising, and grading 12 laboratory projects. Students used **Verilog** in **Active-HDL** for CPU design and implementation.